Abstracts

InP heterojunction bipolar transistor decision circuits

L. Samoska, R. Pullela, B. Agarwal, D. Mensa, Q. Lee, V. Kaman, J. Guthrie and M.J. Rodwell. "InP heterojunction bipolar transistor decision circuits." 1998 MTT-S International Microwave Symposium Digest 98.3 (1998 Vol. III [MWSYM]): 1843-1846.

We have designed and built 30 Gb/s master-slave D-flip-flop circuits using InGaAs-InAlAs HBT's. The HBT devices have a /spl beta/ of 30, and f/sub max/ and f, of 160 and 106 GHz, respectively. We discuss methods of testing decision circuits when bit error rate testing is not available at high data rates.

❑ Return to main document.